

INTERPOLATION FILTER DESIGN ON FPGA



Description of the internship:

The intern will join the design team and contribute to the design of data acquisition system. The intern will be in charge of the development, verification, integration and validation of interpolation filter IP on Xilinx's Spartan-3A FPGA, which is used in multiple designs.

Tasks:

- Deep analysis of design and verification documentations of existing systems,
- Coding of the component in VHDL,
- Coding of the test bench in VHDL,
- RTL Verification by using Modelsim Xilinx Edition,
- Integration of the component in system,
- Validation of the system,
- Redaction of the documentation.

Tools:

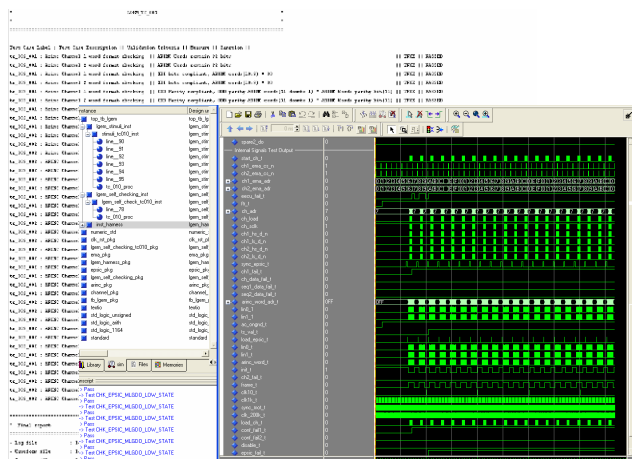
- Language: VHDL, TCL,
- Simulation tool: Modelsim XE©
- EDA tool: ISE Foundation
- Source management: SVN

Profile: Digital HW.

Nb of positions: 1

Opening Date: 12th July

Duration: 3 months



CV to be sent in English with GPA (refer the title of the advertisement) to internship10@elsys-eastern.com by July 6th.